



TS27L4C, TS27L4I, TS27L4M

Very low power precision CMOS quad operational amplifiers

Features

- Very low power consumption :10 $\mu\text{A}/\text{op}$
- Output voltage can swing to ground
- Excellent phase margin on capacitive loads
- Unity gain stable
- Two input offset voltage selections

Description

These devices are low-cost, low-power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the ST silicon gate CMOS process allowing an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available enabling the best consumption-speed ratio:

- $I_{CC} = 10 \mu\text{A}/\text{amp}$: TS27L4 (very low power)
- $I_{CC} = 150 \mu\text{A}/\text{amp}$: TS27M4 (low power)
- $I_{CC} = 1 \text{mA}/\text{amp}$: TS274 (standard)

These CMOS amplifiers offer very high input impedance and extremely low input currents. The major advantage versus JFET devices is the very low input current drift with temperature (see [Figure 4](#)).

For enhanced features of TS27L4, the two micropower, rail-to-rail op-amps families, TS93x and TS94x will better suit low voltage applications.

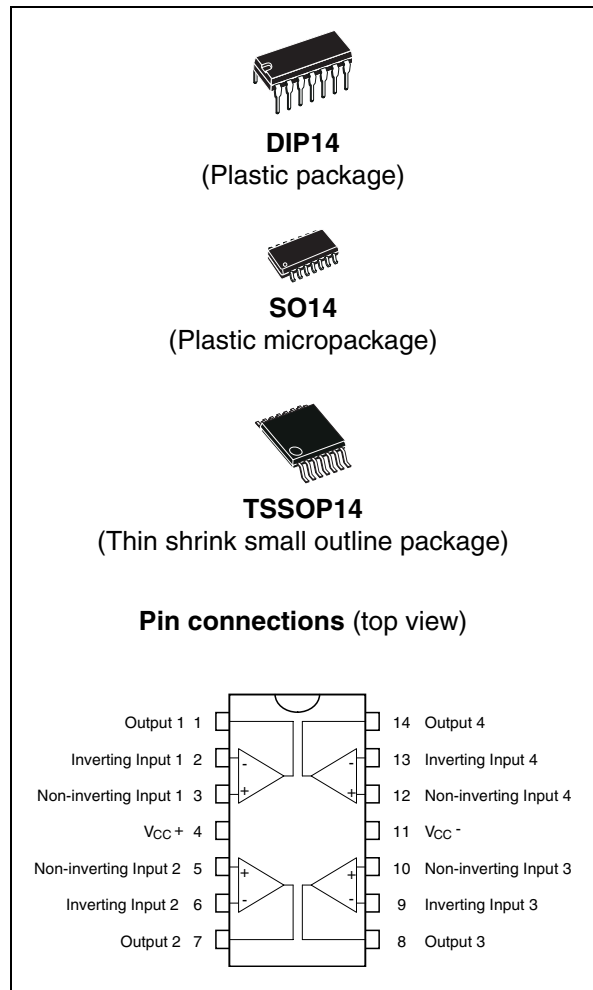


Table 1. Enhanced related families

Part number	V_{CC} range (V)	Rail-to-rail I/O	V_{io} max (mV)	I_{ib} max (μA)	A_{vd} typ (dB)	I_{CC} max (μA)	GBP typ (kHz)	SR typ (V/ms)	Packages
TS944	2.7 - 10	O	2/5/10	150	100	1.85	10	4.5	SO-14, DIP14, TSSOP14
TS934	2.7 - 10	O	2/5/10	150	120	33	100	50	

1 Circuit schematics

Figure 1. Internal block diagram

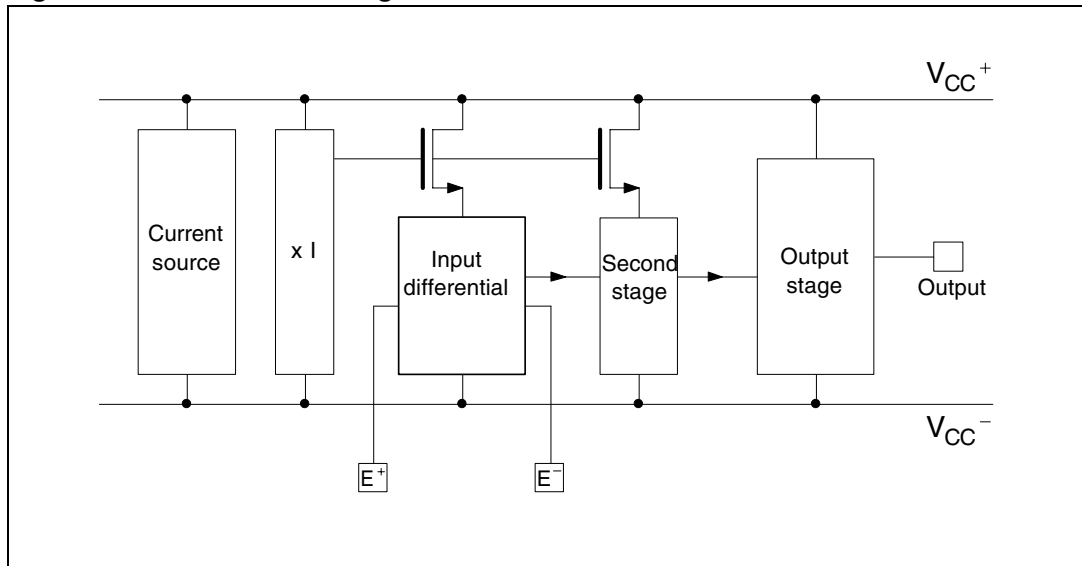
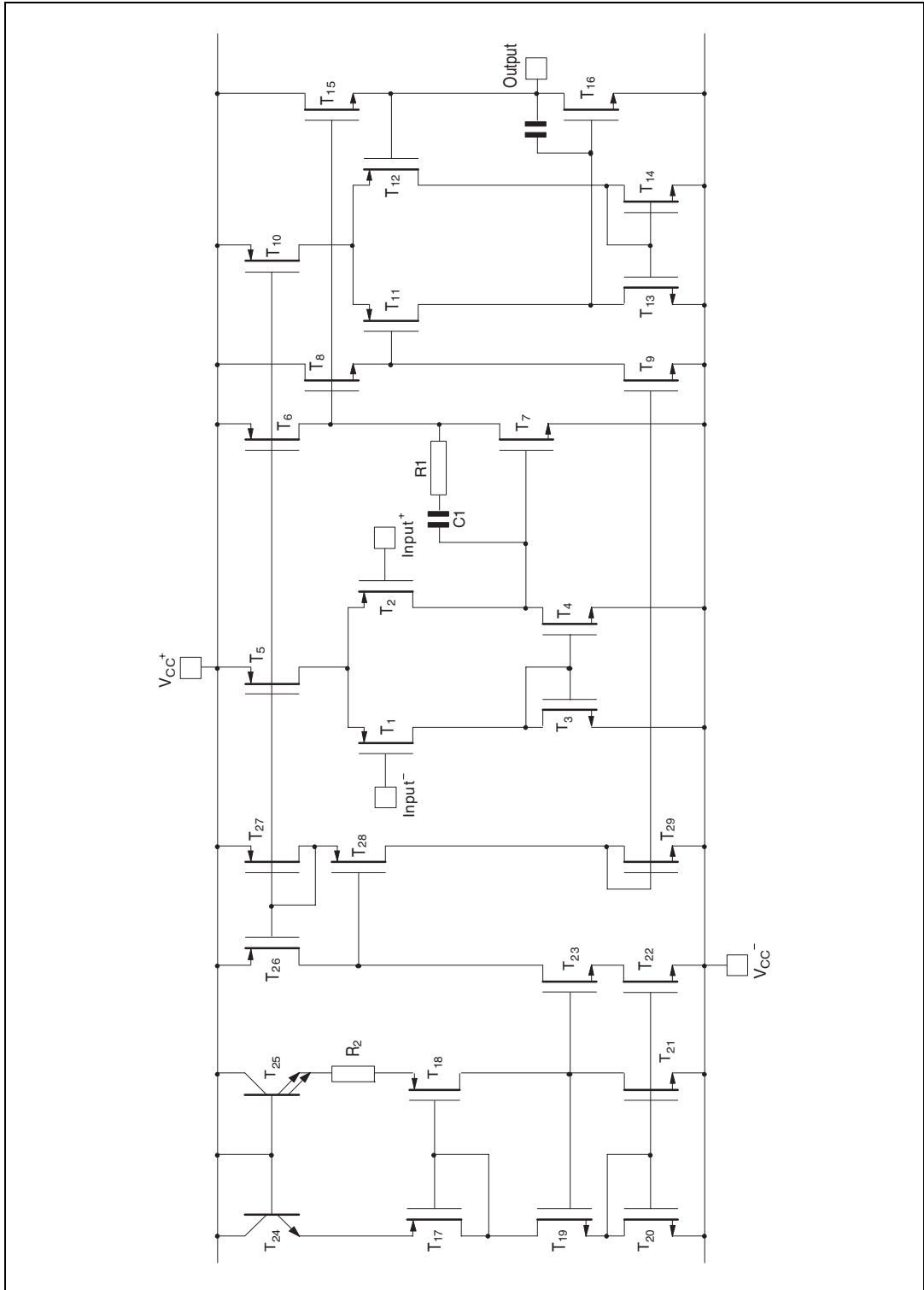


Figure 2. Schematic diagram (for 1/4 TS27L4)



2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings (AMR)

Symbol	Parameter	TS27L4C/AC	TS27L4I/AI	TS27L4M/AM	Unit
V_{CC+}	Supply voltage ⁽¹⁾	18			V
V_{id}	Differential input voltage ⁽²⁾	±18			V
V_{in}	Input voltage ⁽³⁾	-0.3 to 18			V
I_o	Output current for $V_{CC+} \geq 15V$	±30			mA
I_{in}	Input current	±5			mA
T_{oper}	Operating free-air temperature range	0 to +70	-40 to +125	-55 to +125	°C
T_{stg}	Storage temperature range	-65 to +150			°C
R_{thja}	Thermal resistance junction to ambient ⁽⁴⁾				°C/W
	SO-14	105			
	TSSOP14	100			
R_{thjc}	Thermal resistance junction to case ⁽⁴⁾				°C/W
	SO-14	31			
	TSSOP14	32			
ESD	HBM: human body model ⁽⁵⁾	1			kV
	MM: machine model ⁽⁶⁾	100			V
	CDM: charged device model ⁽⁷⁾	1.5			kV

- All values, except differential voltage are with respect to network ground terminal.
- Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
- The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.
- Short-circuits can cause excessive heating and destructive dissipation. Values are typical.
- Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
- Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω). This is done for all couples of connected pin combinations while the other pins are floating.
- Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC+}	Supply voltage	3 to 16	V
V_{icm}	Common mode input voltage range	0 to $V_{CC+} - 1.5$	V

3 Electrical characteristics

Table 4. $V_{CC}^+ = +10V$, $V_{CC}^- = 0V$, $T_{amb} = +25^\circ C$ (unless otherwise specified)

Symbol	Parameter	TS27L4C/AC			TS27L4I/All TS27L4M/AM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input offset voltage $V_o = 1.4V$, $V_{ic} = 0V$ TS27L4		1.1	10		1.1	10	mV
	TS27L4A		0.9	5		0.9	5	
	$T_{min} \leq T_{amb} \leq T_{max}$ TS27L4			12			12	
	TS27L4A			6.5			6.5	
DV_{io}	Input offset voltage drift		2			2		$\mu V/^\circ C$
I_{io}	Input offset current ⁽¹⁾ $V_{ic} = 5V$, $V_o = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		1			1		pA
				100			200	
I_{ib}	Input bias current ⁽¹⁾ $V_{ic} = 5V$, $V_o = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		1			1		pA
				150			300	
V_{OH}	High level output voltage $V_{id} = 100mV$, $R_L = 1M\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$	8.8	9		8.8	9		V
		8.7			8.6			
V_{OL}	Low level output voltage $V_{id} = -100mV$			50			50	mV
A_{vd}	Large signal voltage gain $V_{ic} = 5V$, $R_L = 1M\Omega$, $V_o = 1V$ to $6V$ $T_{min} \leq T_{amb} \leq T_{max}$	60	100		60	100		V/mV
		45			40			
GBP	Gain bandwidth product $A_v = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$, $f_{in} = 100kHz$		0.1			0.1		MHz
CMR	Common mode rejection ratio $V_{ic} = 1V$ to $7.4V$, $V_o = 1.4V$	65	80		65	80		dB
SVR	Supply voltage rejection ratio $V_{CC}^+ = 5V$ to $10V$, $V_o = 1.4V$	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ $T_{min} \leq T_{amb} \leq T_{max}$		10	15		10	15	μA
				17			18	
I_o	Output short circuit current $V_o = 0V$, $V_{id} = 100mV$		60			60		mA
I_{sink}	Output sink current $V_o = V_{CC}$, $V_{id} = -100mV$		45			45		mA
SR	Slew rate at unity gain $R_L = 1M\Omega$, $C_L = 100pF$, $V_i = 3$ to $7V$		0.04			0.04		V/ μs

Table 4. $V_{CC^+} = +10V$, $V_{CC^-} = 0V$, $T_{amb} = +25^{\circ}C$ (unless otherwise specified) (continued)

Symbol	Parameter	TS27L4C/AC			TS27L4I/All TS27L4M/AM			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
ϕ_m	Phase margin at unity gain $A_V = 40dB$, $R_L = 1M\Omega$, $C_L = 100pF$		45			45		Degrees
K_{OV}	Overshoot factor		30			30		%
e_n	Equivalent input noise voltage $f = 1kHz$, $R_S = 100\Omega$		68			68		$\frac{nV}{\sqrt{Hz}}$
V_{O1}/V_{O2}	Channel separation		120			120		dB

1. Maximum values include unavoidable inaccuracies of the industrial tests.

Typical characteristics

Figure 3. Supply current (each amplifier) versus supply voltage

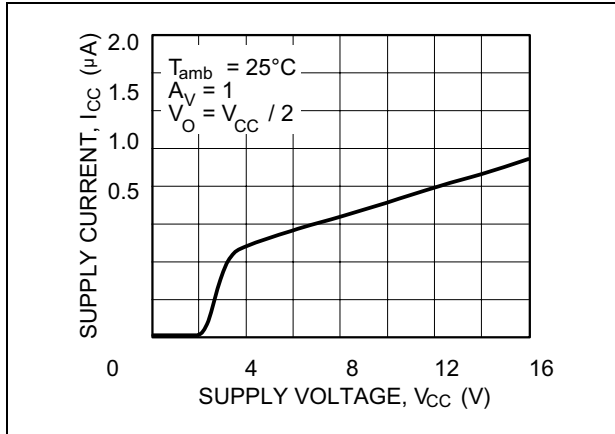


Figure 4. Input bias current versus free air temperature

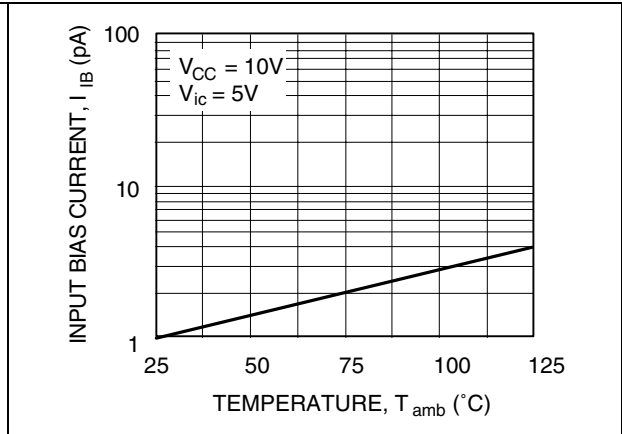


Figure 5. High level output voltage versus high level output current

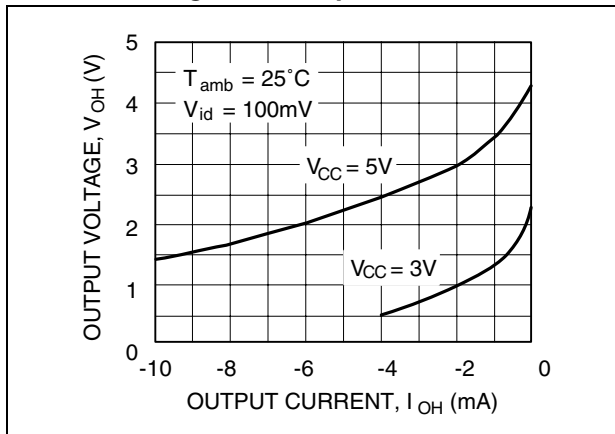


Figure 6. High level output voltage versus high level output current

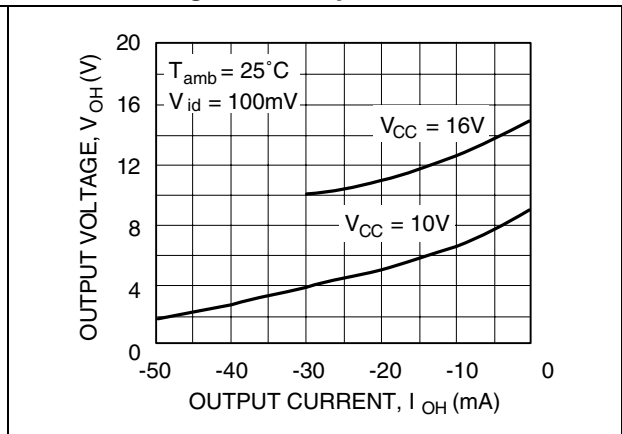


Figure 7. Low level output voltage versus low level output current

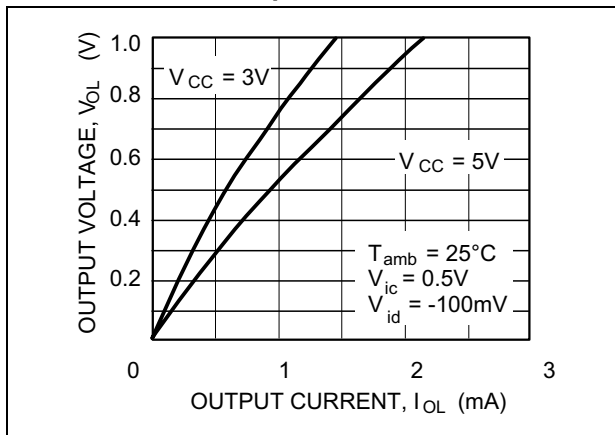


Figure 8. Low level output voltage versus low level output current

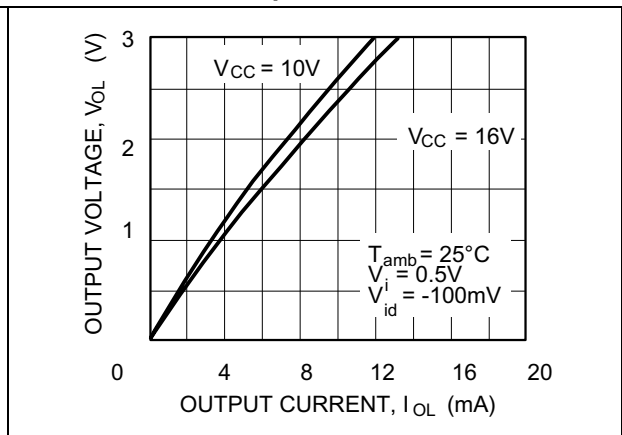


Figure 9. Open loop frequency response and phase shift **Figure 10. Gain bandwidth product versus supply voltage**

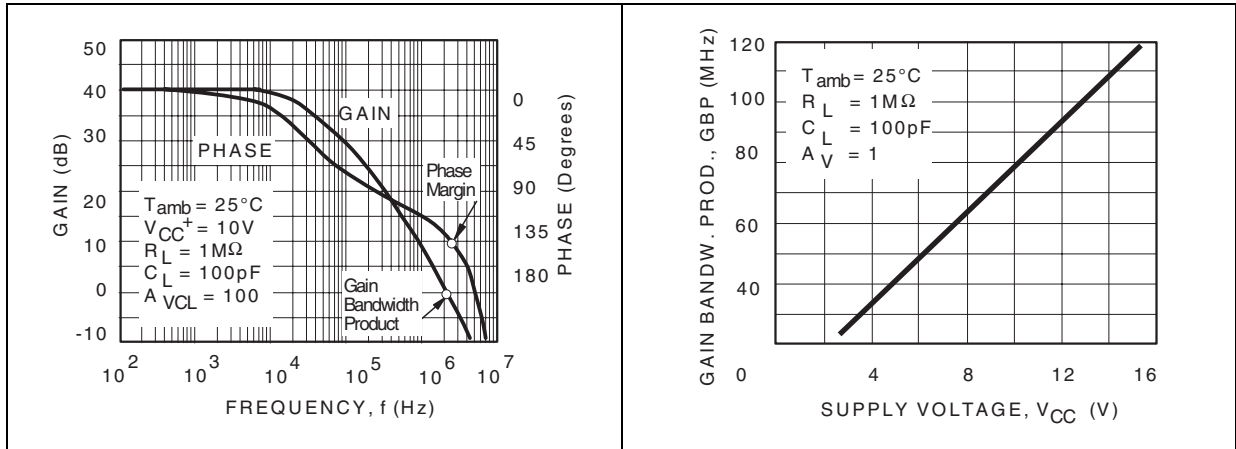


Figure 11. Phase margin versus supply voltage

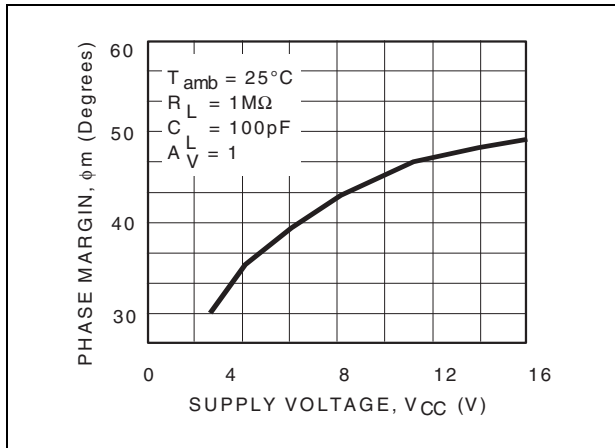


Figure 12. Phase margin versus capacitive load

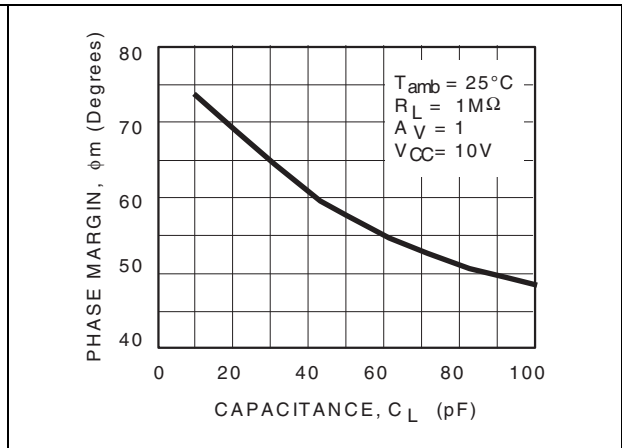


Figure 13. Slew rate versus supply voltage

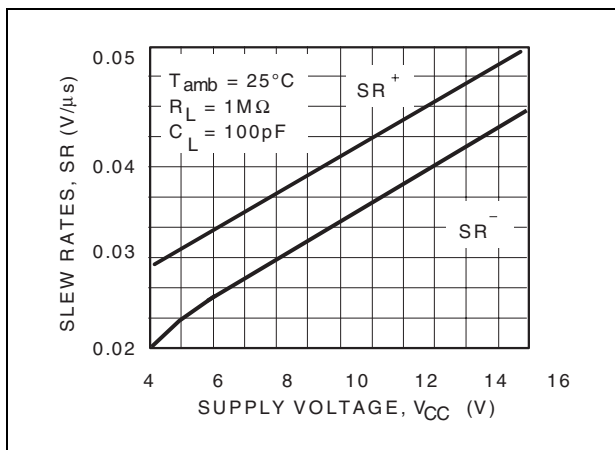
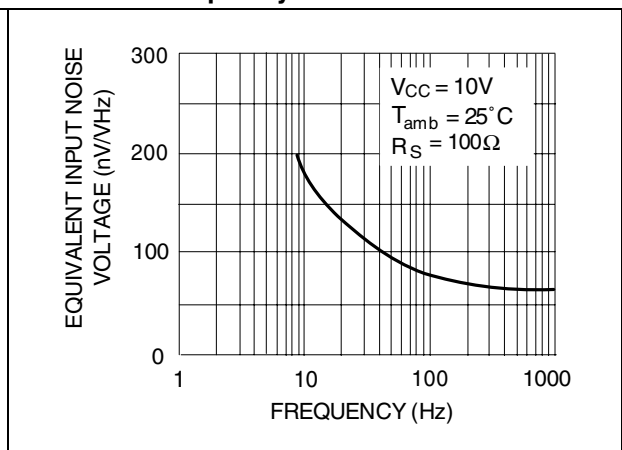


Figure 14. Input voltage noise versus frequency



4 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

4.1 DIP14 package information

Figure 15. DIP14 package mechanical drawing

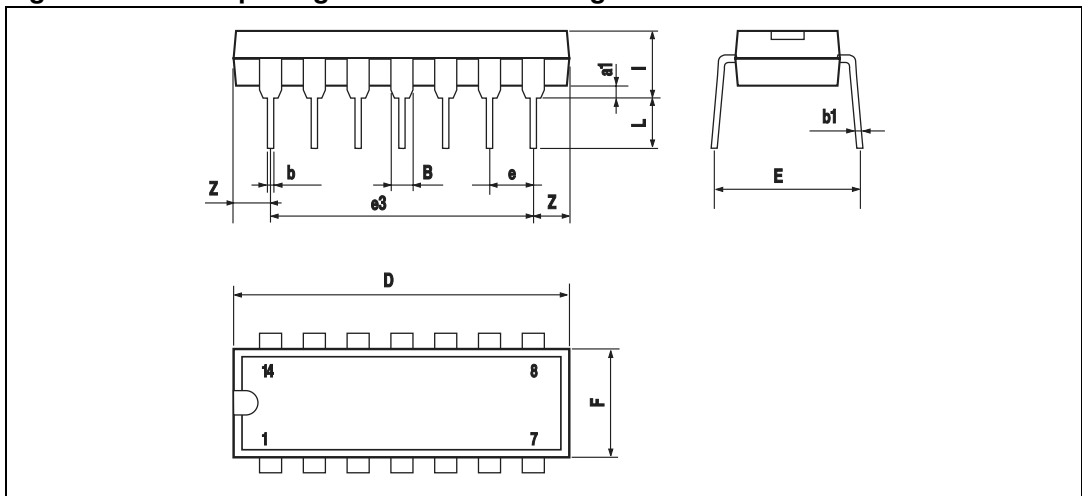


Table 5. DIP14 package mechanical data

Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

4.2 SO-14 package information

Figure 16. SO-14 package mechanical drawing

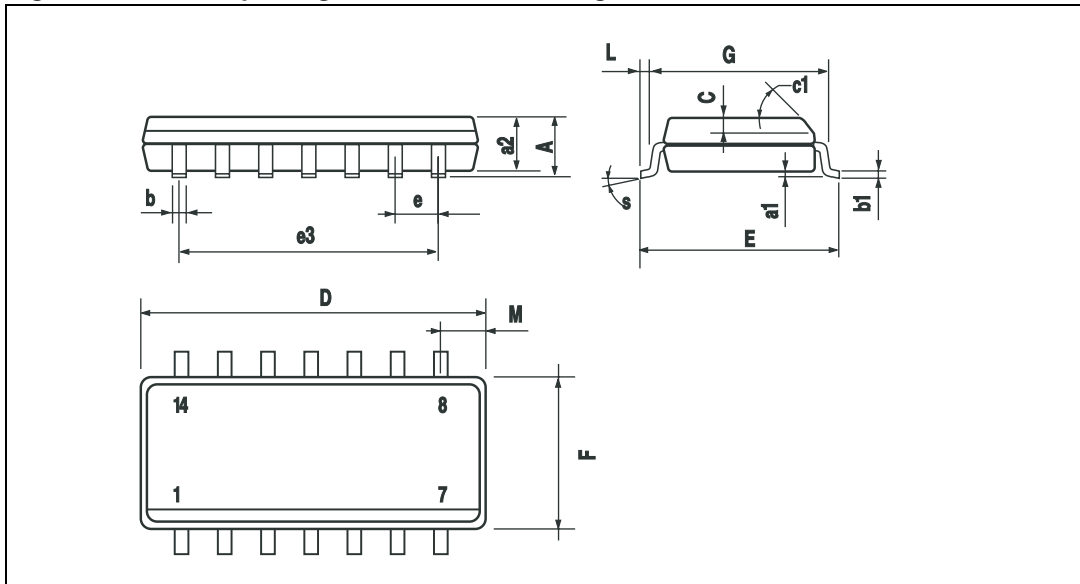


Table 6. SO-14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

4.3 TSSOP14 package information

Figure 17. TSSOP14 package mechanical drawing

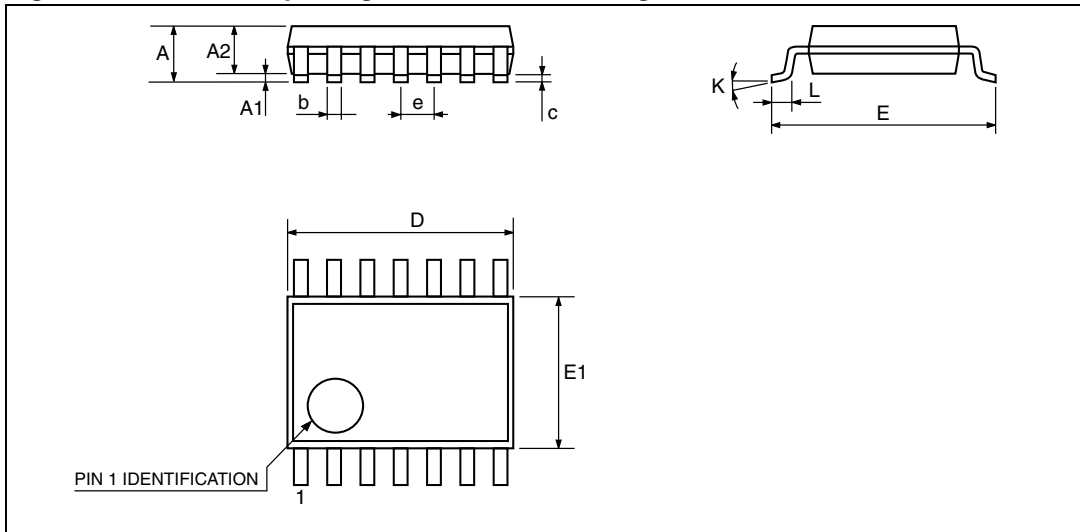


Figure 18. TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L1	0.45	0.60	0.75	0.018	0.024	0.030

5 Ordering information

Table 7. Order codes

Order code	Temperature range	Package	Packing	Marking	
TS27L4CD TS27L4CDT	0°C, +70°C	SO-14	Tube or Tape & reel	27L4C	
TS27L4ACD TS27L4ACDT				27L4AC	
TS27L4CN TS27L4ACN		DIP14	Tube	TS27L4CN	
TS27L4CPT TS27L4ACPT				TS27L4ACN	
TS27L4ID TS27L4IDT	-40°C, +125°C	SO-14	Tube or Tape & reel	27L4C	
TS27L4AID TS27L4AIDT				27L4AC	
TS27L4IN TS27L4AIN		DIP14	Tube	27L4I	
TS27L4IPT TS27L4AIPT				27L4AI	
TS27L4MD TS27L4MDT		-55°C, +125°C	SO-14	Tube or Tape & reel	TS27L4IN
TS27L4AM TS27L4AMDT					TS27L4AIN
TS27L4MN TS27L4AMN	DIP14		Tube	27L4I	
TS27L4MPT TS27L4AMPT				27L4AI	
		TSSOP14	Tape & reel	27L4M	
				27L4AM	

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Nov-2001	1	Initial release.
08-Sep-2008	2	Removed TS27L4B version of device. Added R_{thja} , R_{thjc} , and ESD parameters in Table 2: Absolute maximum ratings (AMR) . Expanded Table 7: Order codes . Updated document format.

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